What is claimed is:

1. A method comprising the steps of:
(a) simulating on a processor a fabrication of a plurality of layout patterns by a lithographic process;
(b) determining sensitivities of the layout patterns to a plurality of parameters based on the simulation;
(c) using the sensitivities to calculate deviations of the patterns across a range of each respective one of the parameters; and
(d) selecting ones of the patterns having predetermined deviation characteristics to be used as test patterns.

2. The method of claim 1, further comprising applying optical proximity correction, and repeating steps (a) through (d).

3. The method of claim 1, wherein step (b) includes calculating the sensitivity of one of the patterns with respect to one of the parameters as a partial derivative of the deviation of the one pattern with respect to the one parameter, based on only two values of the one parameter and the corresponding two values of the deviation of the one pattern.

4. The method of claim 1, wherein step (c) includes calculating the deviations of the patterns using a first degree polynomial that is a linear combination of deviation portions due to each respective parameter, each respective deviation calculated based on the respective sensitivity of the pattern to that parameter.

5. The method of claim 1, further comprising automatically selecting the patterns having maximum or near-maximum deviations to be used as test patterns.

6. The method of claim 5, further comprising printing the patterns having maximum or near-maximum deviations on a test chip or test wafer.

7. The method of claim 1, further comprising selecting a plurality of directions, and selecting the respective patterns having the maximum deviation in each respective one of the plurality of directions to be used as test patterns.

8. The method of claim 1, wherein the predetermined deviation characteristics are selected from the group consisting of maximum, near maximum, minimum and near minimum deviations in a multidimensional process parameter space.

9. The method of claim 1, wherein the patterns are selected so as to have extremal sensitivities with respect to deviations in process parameters.

10. A computer-implemented system comprising:

means for simulating on a processor a fabrication of a plurality of layout patterns by a lithographic process;

means for determining sensitivities of the layout patterns to a plurality of parameters based on the simulation;

means for using the sensitivities to calculate deviations of the patterns across a range of each respective one of the parameters; and

means for selecting ones of the patterns having predetermined deviation characteristics to be used as test patterns.

11. A computer-readable medium encoded with computer program code, wherein, when the computer program code is executed by a processor, the processor performs a method comprising the steps of:

(a) simulating on a processor a fabrication of a plurality of layout patterns by a lithographic process;

(b) determining sensitivities of the layout patterns to a plurality of parameters based on the simulation;

(c) using the sensitivities to calculate deviations of the patterns across a range of each respective one of the parameters; and

(d) selecting ones of the patterns having predetermined deviation characteristics to be used as test patterns.

12. A computer implemented system comprising:

means for receiving a set of priorities from a user;

means for selecting a subset of features of a mask having the highest error rates, using a plurality of layout data;

means for constructing an extrema map consistent with the user input;

means for identifying one or more changes to the layout data based on the extrema map.

13. The system of claim 12, further comprising means for systematically selecting characterizing structures from a layout that is generated from the layout data, the characterizing structures characterizing the lithography and process performance of the layout.

14. The system of claim 13, wherein the selecting of characterizing structures is based on lithographical properties of the characterizing structures.

15. The system of claim 13, wherein the characterizing structures are selected based on the lithographical properties of the characterizing structures under variation of a plurality of process parameters.

16. The system of claim 15, wherein the selection of characterizing structures includes:

characterizing each process parameter by a respective sensitivity of the pattern to changes of that process parameter; and

selecting a hull of a multi-dimensional process space by combining the sensitivities and determining maximum and/or minimum values of the combined sensitivities.

17. The system of claim 16, wherein a function modeling non-monotonic sensitivity to one of the parameters is defined using sampled extrema points.

18. The system of claim 14, wherein measurements are used to calibrate parameters.

19. The system of claim 18, wherein the measurements are deviations in distance, covered area or critical dimension.

20. An integrated circuit fabricated by a method comprising:

(a) simulating a fabrication of a plurality of layout patterns by a lithographic process;

(b) determining sensitivities of the layout patterns to a plurality of parameters based on the simulation;

(c) selecting ones of the patterns to be used as test patterns based on the sensitivities;

(d) fabricating the selected test patterns in an apparatus that performs the lithographic process;

(e) performing an inspection of the fabricated test patterns;

(f) adjusting the lithographic process based on the inspection; and

(g) fabricating an integrated circuit in the apparatus using the adjusted lithographic process.